I Claim:

1. A method for forming an enhancement mode p-channel memory cell, comprising:

forming an oxide layer of less than 50 Angstroms (Å) on a substrate having a channel region separating a source and a drain region in the substrate;

forming a floating gate on the oxide layer; and

forming a dielectric layer on the floating gate; and

forming a control gate on the dielectric layer.

2. The method of claim 1, wherein forming the oxide layer includes forming the oxide layer to have a thickness of 23 Angstroms (Å).

3. The method of claim 1, wherein forming the floating gate includes forming a floating gate which is adapted to hold a charge on the order of 10^{-17} Coulombs for longer than 10 hours at 20 degrees Celsius.

4. The method of claim 1, wherein forming the floating gate includes forming a floating gate which is adapted to hold a charge of the order of 10^{-17} Coulombs for at least 1.0 second at 85 degrees Celsius.

5. The method of claim 1, wherein forming the floating gate includes forming a floating gate which has a bottom surface area in contact with the oxide layer of approximately 10^{-10} cm^2.

6. The method of claim 1, wherein forming the p-channel memory cell includes forming the p-channel memory cell to operate at a voltage of approximately 1.0 Volts applied to the control gate.

7. A method for forming an enhancement mode p-channel transistor, comprising:

forming an oxide layer of less than 50 Angstroms (Å) on a substrate having a channel region separating a source and a drain region in the substrate; and

forming a floating gate on the oxide layer, and wherein forming the floating gate includes forming a floating gate which is adapted to hold a charge on the order of 10^{-7} Coulombs for longer than 1.0 hour at 20 degrees Celsius.

8. The method of claim 7, wherein forming an oxide layer of less than 50 Angstroms (Å) includes forming the oxide layer to have a thickness of 23 Angstroms (Å).

9. The method of claim 7, wherein forming the floating gate further includes forming a floating gate which is adapted to hold a charge on the order of 10^{-7} Coulombs for at least 1.0 second at 85 degrees Celsius.

10. The method of claim 7, wherein forming the p-channel transistor further includes forming an intergate dielectric on the floating gate and forming a control gate on the intergate dielectric.

11. The method of claim 7, wherein forming the p-channel transistor includes forming the p-channel transistor to have an operating voltage of less than 2.5 Volts across the oxide layer.

12. A method of forming a memory device, comprising:

forming a plurality of memory cells, wherein forming the plurality of memory cells includes forming at least one p-channel memory cell, and wherein forming at least one p-channel memory cell includes:

forming an oxide layer of less than 50 Angstroms (Å) on a substrate having a channel region separating a source and a drain region in the substrate; and

forming a floating gate on the oxide layer, and wherein forming the floating gate includes forming a floating gate which is adapted to hold a charge on the order of 10^{-17} Coulombs for longer than 1.0 hour at 20 degrees Celsius.; and

forming at least one sense amplifier, wherein forming at least one sense amplifier includes coupling the at least one amplifier to the plurality of memory cells.

13. The method of claim 12, wherein forming an oxide layer of less than 50 Angstroms (Å) includes forming the oxide layer to have a thickness of 23 Angstroms (Å).

14. The method of claim 12, wherein forming the floating gate further includes forming a floating gate which is adapted to hold a charge on the order of 10^{-17} Coulombs for at least 1.0 second at 85 degrees Celsius.

15. The method of claim 12, wherein forming the p-channel transistor further includes forming an intergate dielectric on the floating gate and forming a control gate on the intergate dielectric.

16. The method of claim 15, wherein forming the p-channel transistor further includes forming the p-channel transistor to have an operating voltage of approximately 1.0 Volt on the control gate.

17. The method of claim 12, wherein forming the p-channel transistor includes forming the p-channel transistor to have an operating voltage of less than 2.5 Volts across the oxide layer.

18. A method for forming an enhancement mode p-channel transistor, comprising:

forming an oxide layer of approximately 23 Angstroms (Å) on a substrate having a channel region separating a source and a drain region in the substrate; and

forming a floating gate on the oxide layer, wherein forming the floating gate includes forming a floating gate which is adapted to hold a charge on the order of 10^{-17} Coulombs for at least one second at 85 degrees Celsius.

19. The method of claim 18, further including forming a heavily doped p-type source region and a heavily doped p-type drain region.

20. The method of claim 19, wherein forming a heavily doped p-type source region and a heavily doped p-type drain region includes forming the heavily doped p-type source region and the heavily doped p-type drain region in a n-type well.

21. A method for forming an enhancement mode p-channel transistor, comprising:

forming an oxide layer of approximately 23 Angstroms (Å) on a substrate having a channel region separating a source and a drain region in the substrate;

forming a floating gate on the oxide layer

forming a dielectric layer on the floating gate; and

forming a control gate on the dielectric layer, wherein forming the enhancement mode p-channel transistor includes forming the enhancement mode p-channel transistor to have an operating voltage of less than 2.5 Volts across the oxide layer.

22. The method of claim 21, wherein forming a floating gate on the oxide layer includes forming a p-type polysilicon floating gate.

23. The method of claim 21, wherein forming a floating gate on the oxide layer includes forming a p-type polysilicon-germanium floating gate.

24. A method for forming an enhancement mode p-channel memory cell, comprising:

forming an oxide layer of less than 50 Angstroms (Å) on a substrate having a channel region separating a source and a drain region in the substrate;

forming a floating gate on the oxide layer;

forming a dielectric layer on the floating gate; and

forming a control gate on the dielectric layer, wherein forming the enhancement mode p-channel includes forming the enhancement mode p-channel adapted to have a reliability of an number of cycles of performance of approximately 10^{15} cycles over a lifetime of the enhancement mode p-channel memory cell.

25. The method of claim 24, wherein forming a dielectric layer on the floating gate includes forming a layer of silicon dioxide.

26. The method of claim 24, wherein forming a dielectric layer on the floating gate includes forming a layer of silicon nitride.

27. A method for forming an enhancement mode p-channel memory cell, comprising:

forming an oxide layer of less than 50 Angstroms (Å) on a substrate having a channel region separating a source and a drain region in the substrate;

forming a floating gate on the oxide layer;

forming a dielectric layer on the floating gate; and

forming a control gate on the dielectric layer, wherein forming the enhancement mode p-channel includes forming the enhancement mode p-channel adapted to have a reliability of an number of cycles of performance of

approximately 10^{12} cycles over a lifetime of the enhancement mode p-channel memory cell.

28. The method of claim 27, wherein forming a floating gate on the oxide layer includes forming a heavily doped n-type polysilicon floating gate.

29. The method of 27, wherein forming a floating gate on the oxide layer includes forming a floating gate which has a bottom surface area in contact with the oxide layer of approximately 10^{-10} cm^2.

30. A method for forming an enhancement mode p-channel memory cell, comprising:

forming an oxide layer of about 30 Angstroms (Å) on a substrate having a channel region separating a source and a drain region in the substrate;

forming a floating gate on the oxide layer;

forming a dielectric layer on the floating gate; and

forming a control gate on the dielectric layer, wherein forming the enhancement mode p-channel transistor includes forming the enhancement mode p-channel transistor to have an operating voltage of about 3.0 Volts across the oxide layer.

31. The method of 30, wherein forming a floating gate on the oxide layer includes forming a floating gate which has a bottom surface area in contact with the oxide layer of approximately 10^{-10} cm^2.

32. The method of claim 30, wherein forming a floating gate on the oxide layer includes forming a floating gate which is adapted to hold a charge on the order of 10^{-17} Coulombs for longer than 1.0 hour at 20 degrees Celsius.

33. A method of forming a memory device, comprising:

forming a plurality of memory cells, wherein forming the plurality of memory cells includes forming at least one p-channel memory cell, and wherein forming at least one p-channel memory cell includes:

forming an oxide layer of about 23 Angstroms (Å) on a substrate having a channel region separating a source and a drain region in the substrate;

forming a floating gate on the oxide layer

forming a dielectric layer on the floating gate; and

forming a control gate on the dielectric layer, wherein forming the enhancement mode p-channel transistor includes forming the enhancement mode p-channel transistor to have an operating voltage of approximately 1.0 Volts applied to the control gate; and

forming at least one sense amplifier, wherein forming at least one sense amplifier includes coupling the at least one amplifier to the plurality of memory cells.

34. The method of claim 33, wherein forming a floating gate on the oxide layer includes forming a floating gate which is adapted to hold a charge on the order of 10^{-17} Coulombs for longer than 1.0 hour at 20 degrees Celsius.

35. The method of claim 33, wherein forming a floating gate on the oxide layer includes forming a floating gate which is adapted to hold a charge on the order of 10^{-17} Coulombs for at least one second at 85 degrees Celsius.